Jumpers and Headers Setting Guide

NUCS-PTL

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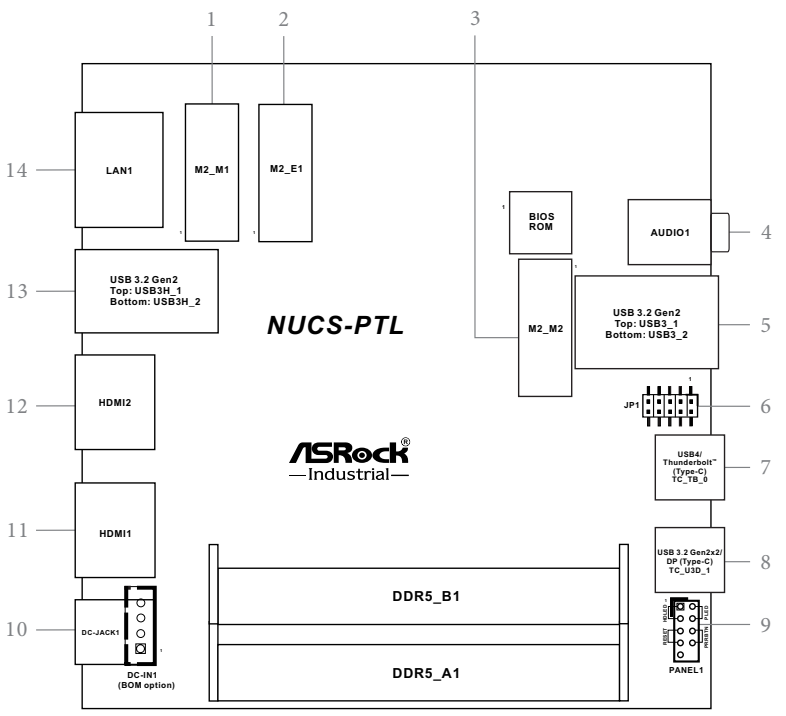
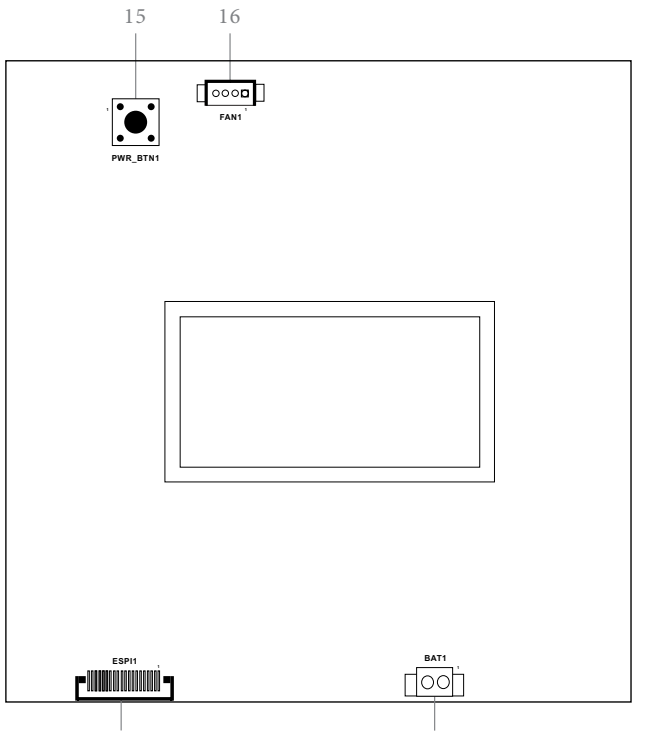
Revision History

Date	Description
July 2, 2025	First Release
September 12, 2025	Second Release

Top:



Bottom:



M.2 Key-M Sockets

1 : M2_M1

Pin	Signal Name	Signal Name	Pin
1	GND	+3.3V	2
3	GND	+3.3V	4
5	PERn3	NA	6
7	PERp3	NA	8
9	GND	SATA_LED	10
11	PETn3	+3.3V	12
13	PETp3	+3.3V	14
15	GND	+3.3V	16
17	PERn2	+3.3V	18
19	PERp2	NA	20
21	GND	NA	22
23	PETn2	NA	24
25	PETp2	NA	26
27	GND	NA	28
29	PERn1	NA	30
31	PERp1	GND	32
33	GND	USB_D+	34
35	PETn1	USB_D-	36
37	PETp1	GND	38
39	GND	NA	40
41	PERn0	NA	42
43	PERp0	NA	44
45	GND	NA	46
47	PETn0	NA	48
49	PETP0	PERST#	50
51	GND	CLKREQ#	52
53	PEFCLKn	NA	54
55	PEFCLKp	NA	56
57	GND	NA	58
67	NA	NA	68
69	PEDET	+3.3V	70
71	GND	+3.3V	72
73	GND	+3.3V	74
75	GND		

3 : M2_M2

Pin	Signal Name	Signal Name	Pin
1	GND	+3.3V	2
3	GND	+3.3V	4
5	NA	NA	6
7	NA	NA	8
9	GND	LED	10
11	NA	+3.3V	12
13	NA	+3.3V	14
15	GND	+3.3V	16
17	NA	+3.3V	18
19	NA	NA	20
21	GND	NA	22
23	NA	NA	24
25	NA	NA	26
27	GND	NA	28
29	NA	NA	30
31	NA	GND	32
33	GND	USB_D+	34
35	NA	USB_D-	36
37	NA	GND	38
39	GND	NA	40
41	PERn0	NA	42
43	PERp0	NA	44
45	GND	NA	46
47	PETn0	NA	48
49	PETP0	PERST#	50
51	GND	CLKREQ#	52
53	PEFCLKn	NA	54
55	PEFCLKp	NA	56
57	GND	NA	58
67	NA	NA	68
69	PEDET	+3.3V	70
71	GND	+3.3V	72
73	GND	+3.3V	74
75	GND		

2 : M.2 Key-E Socket (M2_E1)

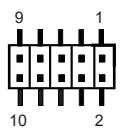
Pin	Signal Name	Signal Name	Pin
1	GND	+3.3V	2
3	USB_D+	+3.3V	4
5	USB_D-	NA	6
7	GND	NA	8
9	CNV_WGR_D1-	CNV_RF_RESET	10
11	CNV_WGR_D1+	NA	12
13	GND	MODEM_CLKREQ	14
15	CNV_WGR_D0-	NA	16
17	CNV_WGR_D0+	GND	18
19	GND	NA	20
21	CNV_WGR_CLK-	CNV_BRI_RSP	22
23	CNV_WGR_CLK+		
		CNV_RGI_DT	32
33	GND	CNV_RGI_RSP	34
35	PETp	CNV_BRI_DT	36
37	PETn	CL_RST#	38
39	GND	CL_DATA	40
41	PERp	CL_CLK	42
43	PERn	CNV_PA_ BLANKING	44
45	GND	CNV_MFUART2_ TXD	46
47	PEFCLKp	CNV_MFUART2_ RXD	48
49	PEFCLKn	SUSCLK	50
51	GND	PERST0#	52
53	CLKREQ#	W_DISABLE1#	54
55	NA	W_DISABLE2#	56
57	GND	NA	58
59	CNV_WT_D1-	NA	60
61	CNV_WT_D1+	NA	62
63	GND	NA	64
65	CNV_WT_D0-	NA	66
67	CNV_WT_D0+	NA	68
69	GND	NA	70
71	CNV_WT_CLK-	+3.3V	72
73	CNV_WT_CLK+	+3.3V	74
75	GND		

4 : Combo Audio Jack (AUDIO1)
(HeadPhone + MIC)

5 : USB 3.2 Gen2 Ports (USB3_1_2)

6 : JP1 Header (JP1)

JP1_12 Short : ATX Mode (Default)
JP1_12 Open : AT Mode
JP1_46 : Clear CMOS
JP1_57 : DACC* (Default)
JP1_68: Enable ME override#
Pin 9-10 : Open: Normal
Pin 9-10 : Short: Active Case Open



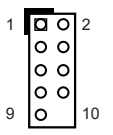
* Auto clear CMOS when system boot improperly.

7 : USB4/Thunderbolt™ Type-C Port (TC_TB_0)

8 : USB 3.2 Gen2x2/DP Type-C Port (TC_U3D_1)

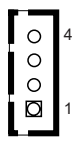
9 : System Panel Header (PANEL1)

Pin	Signal Name	Signal Name	Pin
1	HDLED+	PLED+	2
3	HDLED-	PLED-	4
5	GND	PWRBTN#	6
7	RESET#	GND	8
9	+5VSB		10



10 : DC-In Jack (DC_JACK1)
4-pin DC-in Wafer (DC_IN1) (BOM option)

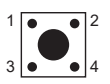
Pin	Signal Name
1	GND
2	DC Input
3	DC Input
4	GND



11 : HDMI Port (HDMI1)
12 : HDMI Port (HDMI2)
13 : USB 3.2 Gen2 Ports (USB3H_1_2)
14 : RJ-45 LAN Port (LAN1)

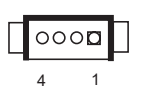
Back Side :

15 : Power Button (PWR_BTN1)



16 : Fan Connector (FAN1)

Pin	Signal Name
1	GND
2	+5V
3	FAN_SPEED
4	FAN_SPEED_CONTROL



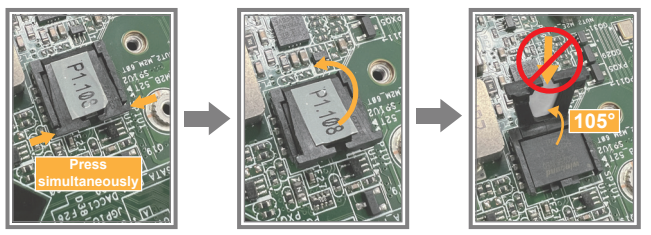
17 : Battery Connector (BAT1)

Pin	Signal Name
1	+BAT
2	GND

18 : ESPI Connector (ESPI)

Pin	Signal Name
1	GND
2	ESPI_CLK
3	GND
4	ESPI_CS#
5	ESPI_RESET#
6	GND
7	+3V
8	GND
9	BUF_PLT_RST#
10	COM_RST#
11	ESPI_IO0
12	ESPI_IO1
13	ESPI_IO2
14	ESPI_IO3
15	GND
16	+3VSB
17	Internal use
18	Internal use
19	ESPI_ALERT#
20	GND

Installation of LOTES ROM Socket



- Do not press one side of the actuator cover at a time. Always apply even and simultaneous force to both sides to avoid damage.
- Do not apply force to the actuator cover after the IC is inserted, especially when it is fully opened at 105 degrees. Pressing vertically at this angle may cause the cover to break.

- The white dot (Pin 1) on the ROM must align with the Pin 1 position of the socket (white arrow area).
- Ensure the white dot on the ROM is facing outward from the socket.

Warning: Incorrect installation may damage the chipset and motherboard. Refer to the picture for proper orientation.